INTRINSIC NOISE CURRENTS IN DEEP SUBMICRON MOSFETS

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ABSTRACT

A systemic extraction method to obtain the induced gate noise ($i_g i_g^*$), channel thermal noise ($i_d i_d^*$) and their cross-correlation term ($i_g i_d^*$) in submicron MOSFETs directly from scattering and RF noise measurements is presented and verified with measurements. The extracted noise currents versus frequency, bias condition and channel length for MOSFETs from a 0.18μm CMOS process are presented and discussed.

INTRODUCTION

Currently, there is a trend to replace RFICs with BJTs and GaAs FETs with deep submicron MOSFETs which have unity current-gain frequencies (f_T) of several tens of GHz [1]. However, for many RFICs, low noise performance is very important. Therefore, RF noise modeling of deep submicron MOSFETs is very important for devices used in the front-end transceivers. Because of the difficulties in the extraction of the induced gate noise and its correlation term with the channel thermal noise, several noise models [2],[3] and simulation results [4] have been presented, but they could not be verified directly with RF noise measurements for deep submicron MOSFETs. In this paper, a systematic procedure to extract the induced gate noise, channel thermal noise and their cross-correlation directly from the scattering and RF noise measurements is presented. The extracted noise currents of the MOSFETs fabricated in a 0.18μm CMOS process versus frequency, bias condition and channel length are presented and discussed.

NOISE SOURCE EXTRACTION

Fig. 1 shows the noise equivalent circuit model of an intrinsic MOSFET that is suitable for RF applications. It consists of two parts - an internal part which consists of C_{GS}, C_{GD}, R_i, g_m, R_{DS}, $i_g i_g^*$ (or i_g^2) and $i_d i_d^*$ (or i_d^2), and an external part which includes all the components outside of the dashed box, such as R_G, C_{GB}, R_S, R_{SB}, R_{DB}, C_{DB} and R_D.

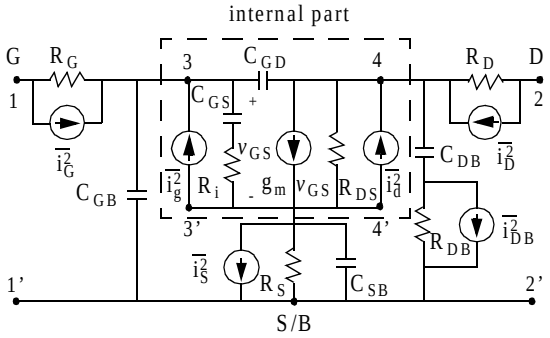

Fig. 1. The RF noise model of an intrinsic MOSFET that is suitable for high-frequency circuit applications.

After the devices and dummy structures, as described in [6], are fabricated, the induced gate noise, channel thermal noise and their correlation in MOSFETs can be extracted by using the following 15-step procedure [7].

1. Measure the scattering parameters $\boldsymbol{S_{DUT}}$, $\boldsymbol{S_{OPEN}}$, $\boldsymbol{S_{THRU1}}$ and $\boldsymbol{S_{THRU2}}$ of the device-under-test (DUT), OPEN, THRU1 and THRU2 dummy structures, respectively [6].
2. Measure the noise parameters (i.e. $NF_{min,DUT}$, $Y_{opt,DUT}$ and $R_{n,DUT}$) of the device-under-test (DUT).
3. Perform the parameter de-embedding to obtain the intrinsic scattering ($\boldsymbol{Y_{dev}}$) and noise parameters ($NF_{min,dev}$, $Y_{opt,dev}$ and $R_{n,dev}$) of the transistor [6].
4. Perform the parameter extraction based on $\boldsymbol{Y_{dev}}$ and other measured data to obtain all the element values (e.g. g_m, C_{GS}, C_{GD},... etc.) in the RF noise equivalent circuit model [8].
5. Calculate the correlation matrix $\boldsymbol{C_{Adev}}$ of the intrinsic transistor as defined in [9],[10].
6. Calculate the four-port admittance matrix $\boldsymbol{Y_{extr}}$ of the external part as defined in Fig. 1 by excluding all noise sources, C_{gs}, C_{gd}, g_m, R_{DS} and R_i, and partition $\boldsymbol{Y_{extr}}$ as

$$\boldsymbol{Y_{extr}} = \begin{bmatrix} \boldsymbol{Y_{ee}} & \boldsymbol{Y_{ei}} \\ \boldsymbol{Y_{ie}} & \boldsymbol{Y_{ii}} \end{bmatrix} \quad (2)$$

where $\boldsymbol{Y_{ee}}$, $\boldsymbol{Y_{ei}}$, $\boldsymbol{Y_{ie}}$ and $\boldsymbol{Y_{ii}}$ are 2×2 matrixes.

7. Calculate the two-port admittance $\boldsymbol{Y_{intr}}$ of the internal part shown in the RF transistor model.
8. Calculate the matrix $\boldsymbol{D}$ as follows [10]

$$\boldsymbol{D} = -\boldsymbol{Y_{ei}}(\boldsymbol{Y_{ii}} + \boldsymbol{Y_{intr}})^{-1}. \quad (3)$$

9. Convert the noise correlation matrix $\boldsymbol{C_{Adev}}$ to $\boldsymbol{C_{Ydev}}$ by

$$\boldsymbol{C_{Ydev}} = \boldsymbol{T_Y}\boldsymbol{C_{Adev}}\boldsymbol{T_Y}^{\dagger} \quad (4)$$

where the † in $\boldsymbol{T_Y}^{\dagger}$ denotes Hermitian conjugation and the transformation matrix $\boldsymbol{T_Y}$ is given by

$$\boldsymbol{T_Y} = \begin{bmatrix} -Y_{11,dev} & 1 \\ -Y_{21,dev} & 0 \end{bmatrix}. \quad (5)$$

10. Calculate the admittance noise correlation matrix $\boldsymbol{C_{Yextr}}$ of the external part by [11]

$$\boldsymbol{C_{Yextr}} = 2kT\Re(\boldsymbol{Y_{extr}}) \quad (6)$$

where $\Re(\ )$ denotes for the real part of the matrix elements, and partition $\boldsymbol{C_{Yextr}}$ as

$$\boldsymbol{C_{Yextr}} = \begin{bmatrix} \boldsymbol{C_{ee}} & \boldsymbol{C_{ei}} \\ \boldsymbol{C_{ie}} & \boldsymbol{C_{ii}} \end{bmatrix} \quad (7)$$

where $\boldsymbol{C_{ee}}$, $\boldsymbol{C_{ei}}$, $\boldsymbol{C_{ie}}$ and $\boldsymbol{C_{ii}}$ are 2×2 matrixes.

11. Calculate the admittance correlation matrix $\boldsymbol{C_{Yintr}}$ of the internal part in Fig. 1 by

$$\boldsymbol{C_{Yintr}} = \boldsymbol{D_i}(\boldsymbol{C_{Ydev}} - \boldsymbol{C_{ee}})\boldsymbol{D_i}^{\dagger} - \boldsymbol{C_{ie}}\boldsymbol{D_i}^{\dagger} - \boldsymbol{D_i}\boldsymbol{C_{ei}} - \boldsymbol{C_{ii}} \quad (8)$$

where $\boldsymbol{D_i} = \boldsymbol{D}^{-1}$.

12. Convert $\boldsymbol{Y_{intr}}$ to its chain representation $\boldsymbol{A_{intr}}$.
13. Convert $\boldsymbol{C_{Yintr}}$ to its chain matrix form $\boldsymbol{C_{Aintr}}$ by using

$$\boldsymbol{C_{Aintr}} = \boldsymbol{T_A}\boldsymbol{C_{Yintr}}\boldsymbol{T_A}^{\dagger}, \quad (9)$$

where $\boldsymbol{T_A}$ is given by

$$\boldsymbol{T_A} = \begin{bmatrix} 0 & A_{12,intr} \\ 1 & A_{22,intr} \end{bmatrix}. \quad (10)$$

14. Calculate the noise parameters, NF_{min}, Y_{opt} and R_n of the internal part in Fig. 1 from the noise correlation matrix $\boldsymbol{C_{Aintr}}$ by the equations (29a) - (29c) in [10].
15. Calculate the power spectral density of the channel thermal noise i_d^2 (or $i_d i_d^*$), induced gate noise i_g^2 (or $i_g i_g^*$) and their cross-correlation term $i_g i_d^*$ by

$$\frac{\overline{|i_d|^2}}{\Delta f} = 4kTR_n|Y_{21,intr}|^2, \quad (11)$$

$$\frac{\overline{|i_g|^2}}{\Delta f} = 4kTR_n\left\{|Y_{opt}|^2 - |Y_{11,intr}|^2 + 2\Re[(Y_{11,intr} - Y_{cor})Y_{11,intr}^*]\right\} \quad \text{and} \quad (12)$$

$$\frac{\overline{i_g i_d^*}}{\Delta f} = 4kT(Y_{11,intr} - Y_{cor})R_n Y_{21,intr}^* \quad (13)$$

where Y_{cor} is given by

$$Y_{cor} = \frac{NF_{min} - 1}{2R_n} - Y_{opt}. \quad (14)$$

MEASUREMENT AND DISCUSSION

The DUTs are n-type MOSFETs fabricated in a 0.18μm CMOS process by Conexant Systems Inc. Measurements were conducted by using an ATN NP5B Noise and S-parameter Measurement Systems (0.3 ~ 6 GHz). All the parasitic effects from probe pads and interconnections were de-embedded. Fig. 2 shows the channel thermal noise versus frequency characteristics for the n-type MOSFETs with channel width W = 10 × 6μm (10 fingers) and lengths L = 0.97μm, 0.64μm, 0.42μm and 0.27μm, respectively, biased at V_{DS} = 1.0 V and V_{GS} = 1.2 V.

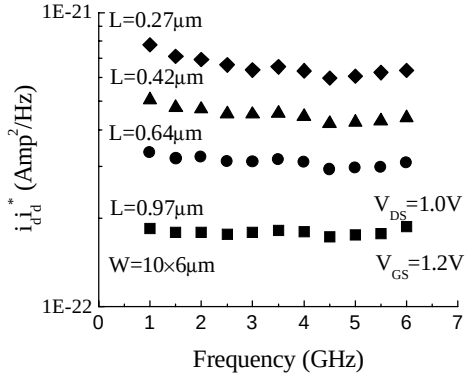

Fig. 2. Extracted channel thermal noise ($i_d i_d^*$) versus frequencies for devices of four different channel lengths.

It is shown that the channel thermal noise, in general, is frequency independent and increases when the channel length decreases. From Figs. 3 and 4, the induced gate noise and the correlation term are proportional to f^2 and f (solid lines), respectively, where f is the operating frequency. In addition, when channel length decreases, both the induced gate noise and the correlation term also decrease.

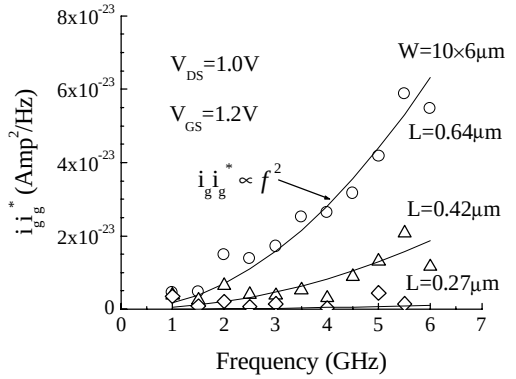

Fig. 3. Extracted induced gate noise ($i_g i_g^*$) versus frequencies for devices of three different channel lengths.

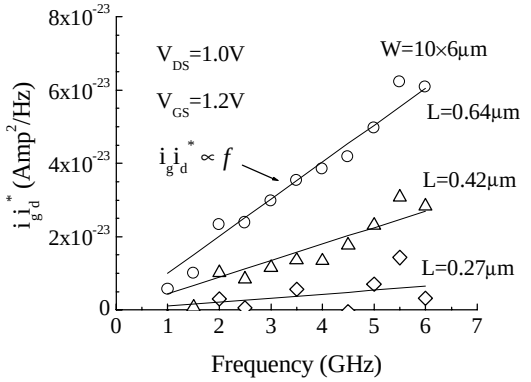

Fig. 4. Extracted cross-correlation term ($i_g i_d^*$) between the induced gate noise and the channel thermal noise versus frequencies for devices of three different channel lengths.

For the bias dependence of the extracted noise currents, Figs. 5, 6 and 7 show the $i_d i_d^*$, $i_g i_g^*$, and $i_g i_d^*$ versus V_{GS} characteristics for the n-type MOSFETs with channel width W = 10 × 6μm and lengths L = 0.97μm, 0.64μm, 0.42μm and 0.27μm, respectively, biased at V_{DS} = 1.0 V. It is shown in Figs. 5 and 7 that $i_d i_d^*$ and $i_g i_d^*$ have a strong bias dependence and they increase when V_{GS} increases then tend to saturate at higher V_{GS} region. From Fig. 6, when V_{GS} increases, $i_g i_g^*$ increases for longer channel devices, but tends to decrease when the channel lengths decrease. It can be explained by the noise model proposed in [3]. For longer channel devices, the induced gate noise is dominant by the one generated in the channel region where the gradual channel approximation holds. The noise from this region tends to increase when V_{GS} increases. However, when the channel lengths decrease, the gate noise generated from the velocity saturation region becomes dominant and it tends to decrease when V_{GS} increases.

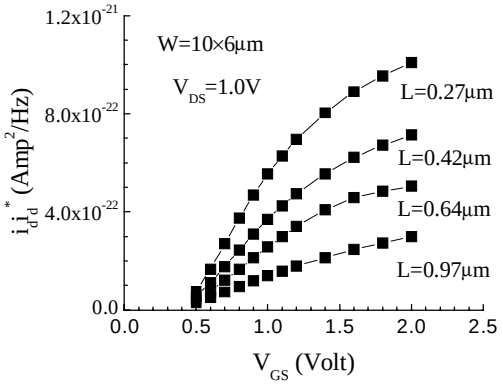

Fig. 5. Extracted channel thermal noise ($i_d i_d^*$) versus V_{GS} characteristics for devices of four different channel lengths.

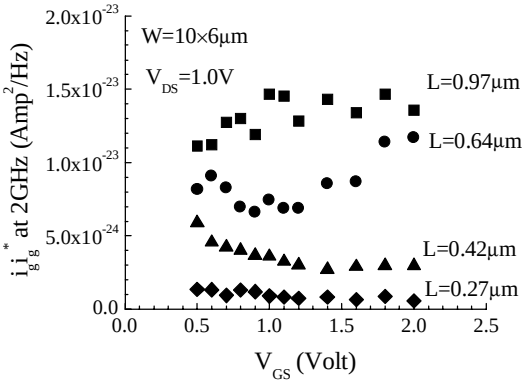

Fig. 6. Extracted induced gate noise ($i_g i_g^*$) versus V_{GS} characteristics for devices of four different channel lengths.

Finally, Figs. 8 and 9 show the ratio of the short-circuited output noise currents generated by $i_g i_g^*$ and $i_g i_d^*$ to that generated by $i_d i_d^*$ with 50Ω source impedance when transistors were biased at V_{DS}=1.0V and V_{GS} = 1.2V. It is shown that $i_g i_d^*$ contributes more noise currents than $i_g i_g^*$ does at the

output port and both of them contribute less than 5% of the output noise current generated by $i_d i_d^*$.

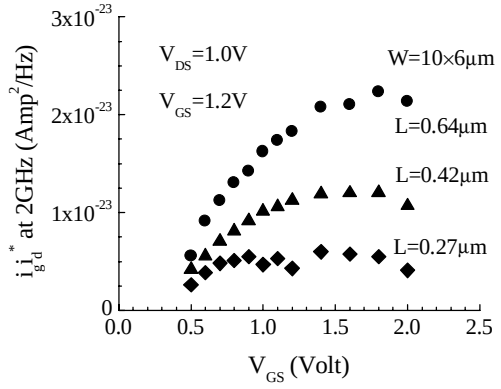

Fig. 7. Extracted cross-correlation term ($i_g i_d^*$) between the induced gate noise and the channel thermal noise versus V_{GS} characteristics for devices of three different channel lengths.

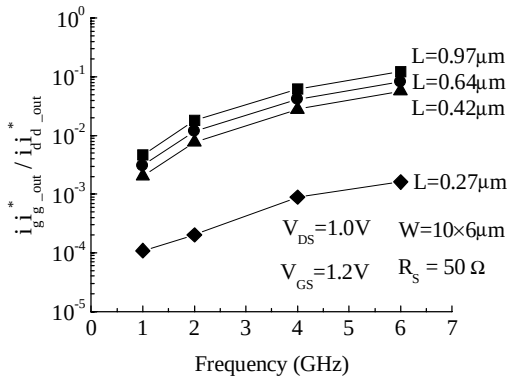

Fig. 8. The ratio of the output noise current from the induced gate noise ($i_g i_{g\_out}^*$) to the output noise from the channel thermal noise ($i_d i_{d\_out}^*$) as a function of frequencies with $R_S = 50\ \Omega$.

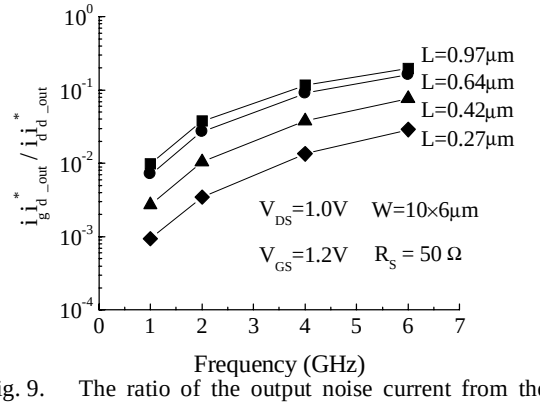

Fig. 9. The ratio of the output noise current from the cross-correlation noise ($i_g i_{d\_out}^*$) to the output noise from the channel thermal noise ($i_d i_{d\_out}^*$) as a function of frequencies with $R_S = 50\ \Omega$.

CONCLUSION

The intrinsic noise sources in MOSFETs extracted from on-wafer scattering and noise measurements have been presented. From the extracted results of all tested devices, the channel thermal noise $i_d i_d^*$ is frequency independent, increases when the channel length decreases for all bias conditions at a fixed V_{DS}, and is the most dominant noise source at the frequencies and bias conditions discussed. On the other hand, $i_g i_g^*$ and $i_g i_d^*$ have small noise contribution at the output port of transistors and less impact for the shorter channel devices. Therefore, an accurate and physics-based noise model for the channel thermal noise is crucial for MOSFETs when modeling RF low noise circuits.

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